technische universität dortmund

CS 12 computer science 12

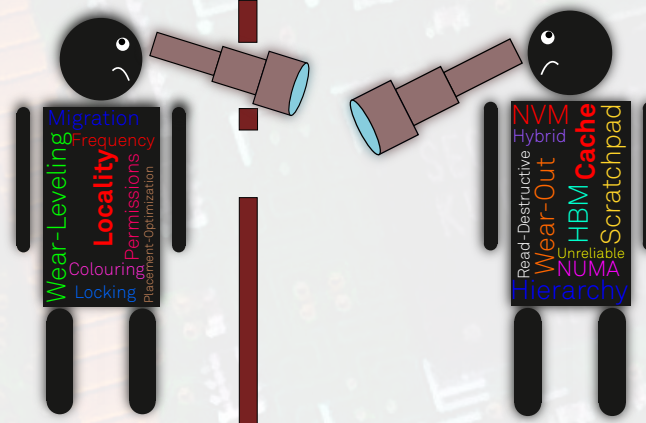Databases and Information Systems Group

Memory Diplomat
Jian-Jia Chen ○ Jens Teubner ○ Roland Kühn
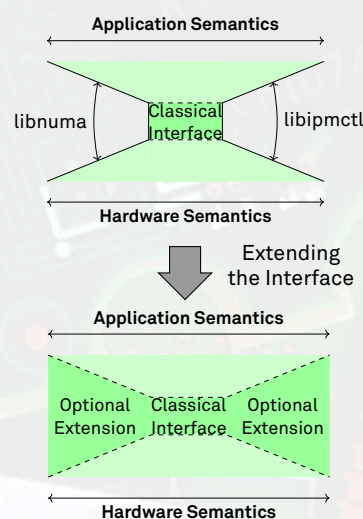
The Problem

- Modern computing systems abstract memory access typically to a very narrow interface

- Characteristics only visible by "punching holes" in the wall that separates Software and Hardware

- Even more challenging with new emerging memory technologies
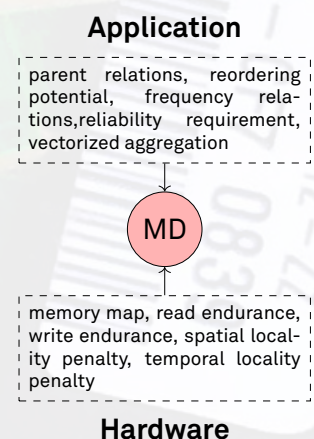
Need to Actively Negoatiate...

Add an Instance for Negotiation between Hardware and Software
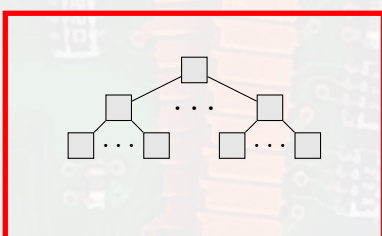→ **Memory Diplomat**

...Over an Extended Interface...

Application Semantics

libnuma — Classical Interface — libipmctl

Hardware Semantics

Extending the Interface

Application Semantics

Optional Extension — Classical Interface — Optional Extension

Hardware Semantics

...by Considering Abstract Behavioral Characteristics

Application

parent relations, reordering potential, frequency relations, reliability requirement, vectorized aggregation

MD

memory map, read endurance, write endurance, spatial locality penalty, temporal locality penalty

Hardware

Example

Application

```
OrderedTree::OrderedTree(){
    MD::registerDataRelation(root,
        root->child[0],
        MD::DataRelation::FollowsProb(0.6));

    MD::allowRemapping(node_list,
        OrderedTree::swapNodeLocation,
        MD::Reordering::ARBITRARY_ORDERING);
    [...]
}
```
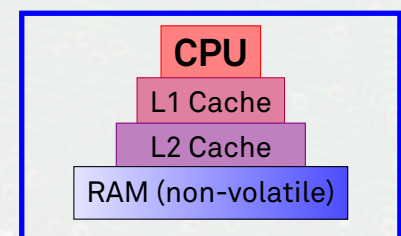
```xml
<cpu>
    <cachelevel>2</cachelevel>
    <l1d-size>32</l1d-size>
    <l1d-cl-size>64</l1d-cl-size>
    ...
</cpu>
<memory>
    ...
    <retention-time>'2y'</retention-time>
</memory>
```

Hardware

Register Chrararacteristics → **Memory Diplomat** ← Register Chrararacteristics

CPU
L1 Cache
L2 Cache
RAM (non-volatile)

Memory Diplomat

- Joint project of the DAES group and the DBIS group at TU Dortmund University

- *Memory Diplomat* is our vision of a modernized memory interface that is able to take characteristics from hardware and application into account.

- *Memory Diplomat* is intended to be easily extendable, enabling an easy integration into other projects within the priority program.

Intended Track

- The plan is to "shape" the *Memory Diplomat* incrementally, covering the following topics over the next three years:

  ○ Memory Lifetime
  ○ Access Sequences
  ○ Hybrid Memory Systems
  ○ Unreliability
  ○ In-Memory Computing

3 Years