

# VAMPIR

## Virtualized Non-Functional Memory Properties for Data-Pipeline Scheduling

### Vision

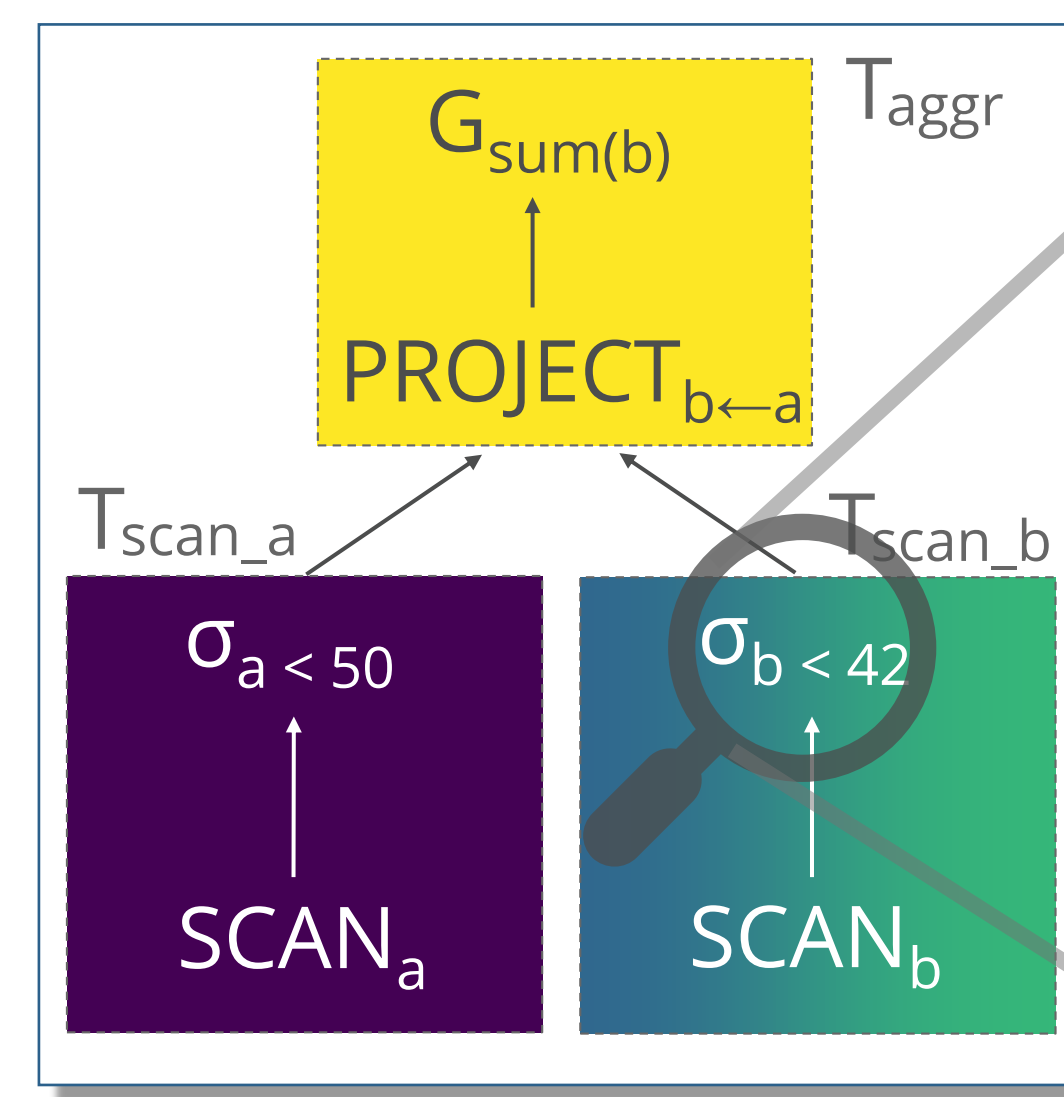
```
void *buffer = vmalloc(buffer_size,
    MP_PERSISTENT |
    MP_THROUGHPUT_HIGH |
    MP_FAULT_TOLERANT,
    WP_READ_90,
    usage_time(0, 30));
```

### Expectations

- Requested Memory Properties and
  - Expected Workload Properties
- Interface allocates best suited available memory

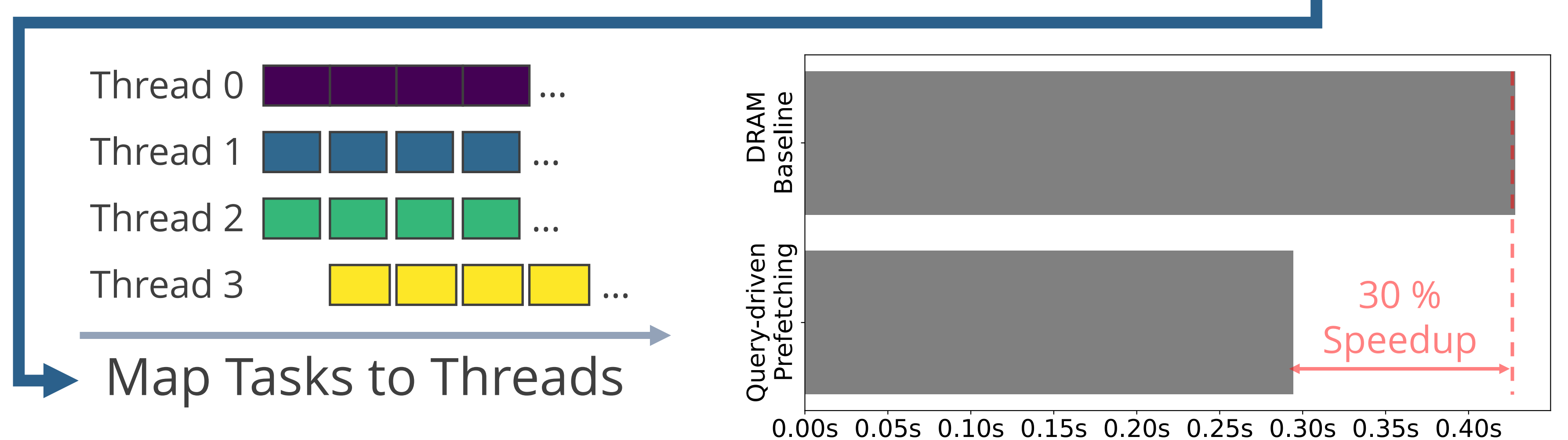
### Intra-Pipeline Optimization – Query-driven Prefetching

```
SELECT sum(b)
FROM r
WHERE a < 50
AND b < 42;
```

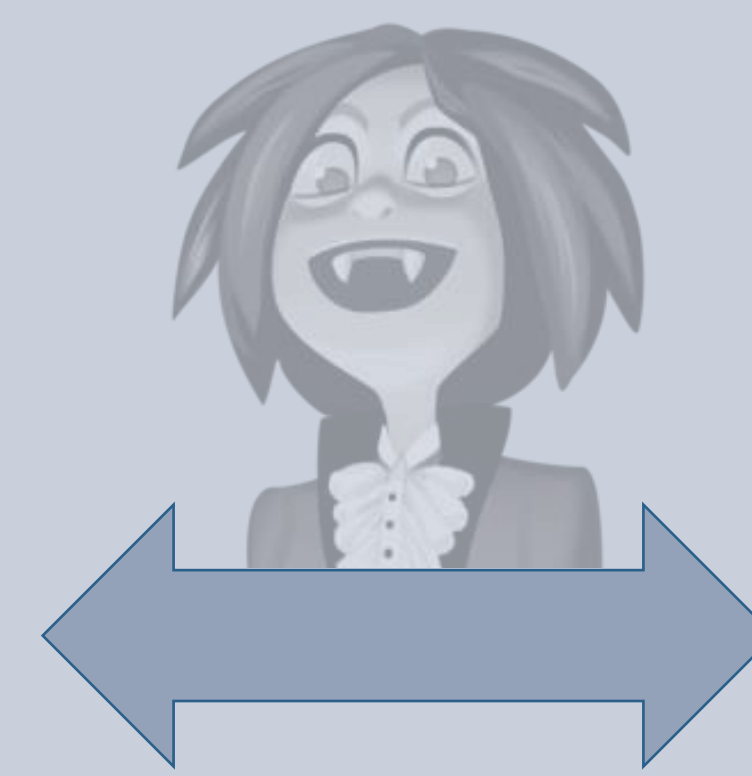
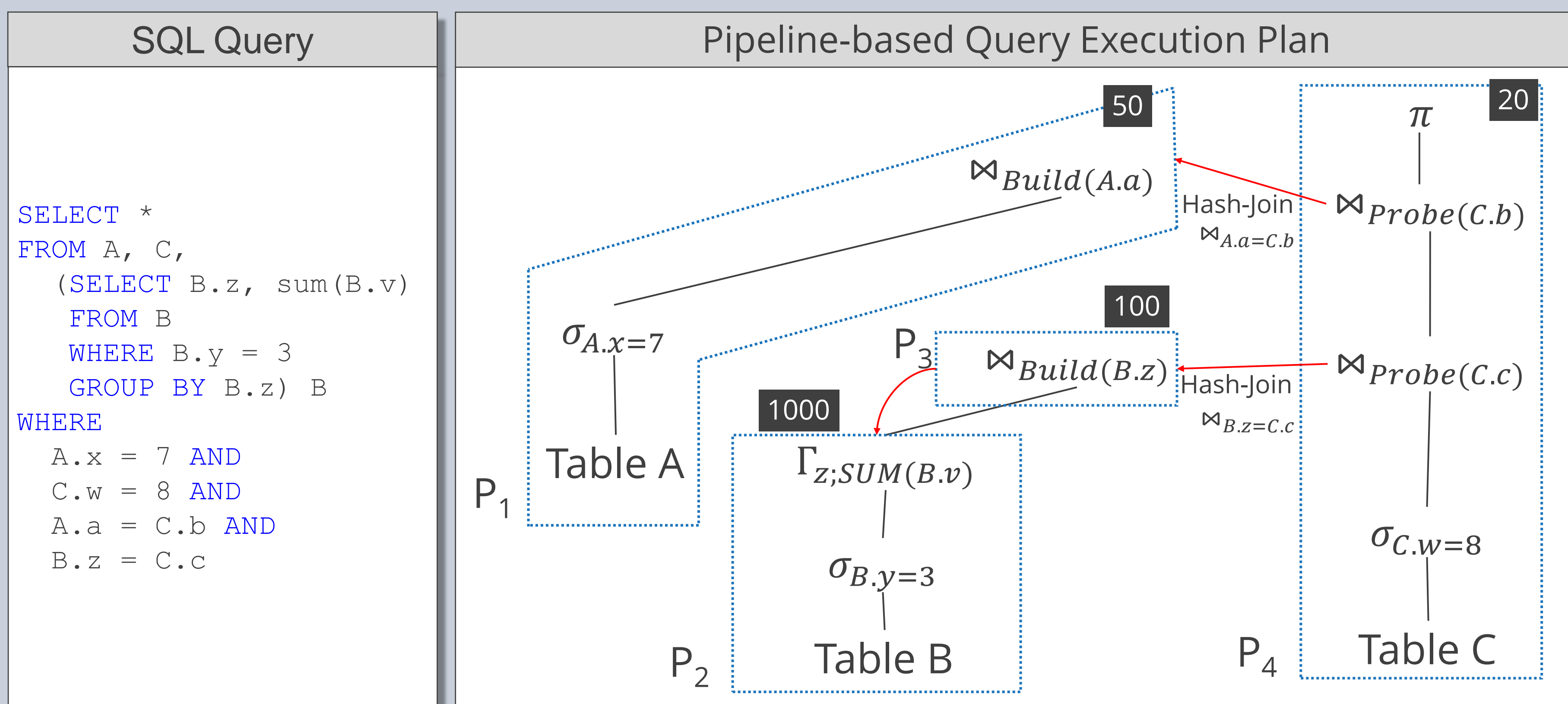


```
label:
value a = load(source);
bool r = compare(a, 42);
store_→addr(r);
store_→hbm(a);
goto label;
```

Calculate Pipeline Execution Plan → Subdivide Plan into Tasks → Find Optimization Potential and inject Store Instructions



## VAMPIR-Project



## Disruptive Memory Technologies

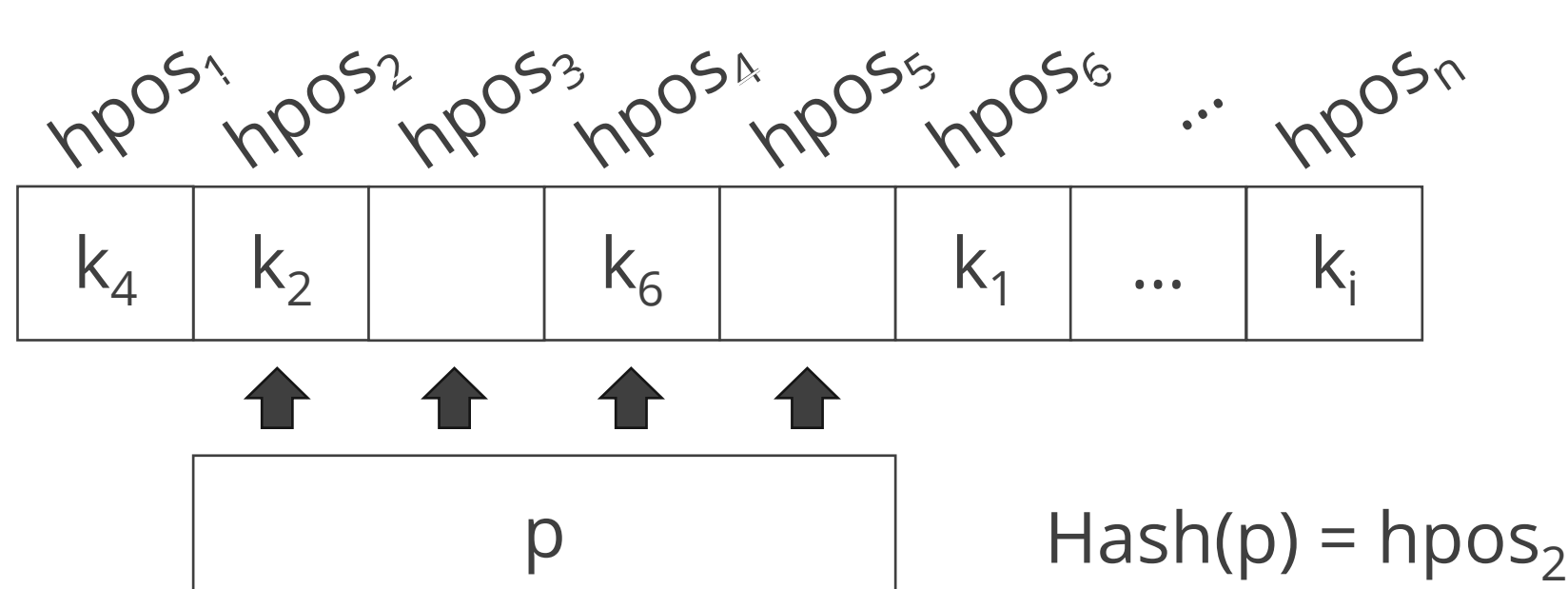
### Central Problem

How to make disruptive memories easily accessible?

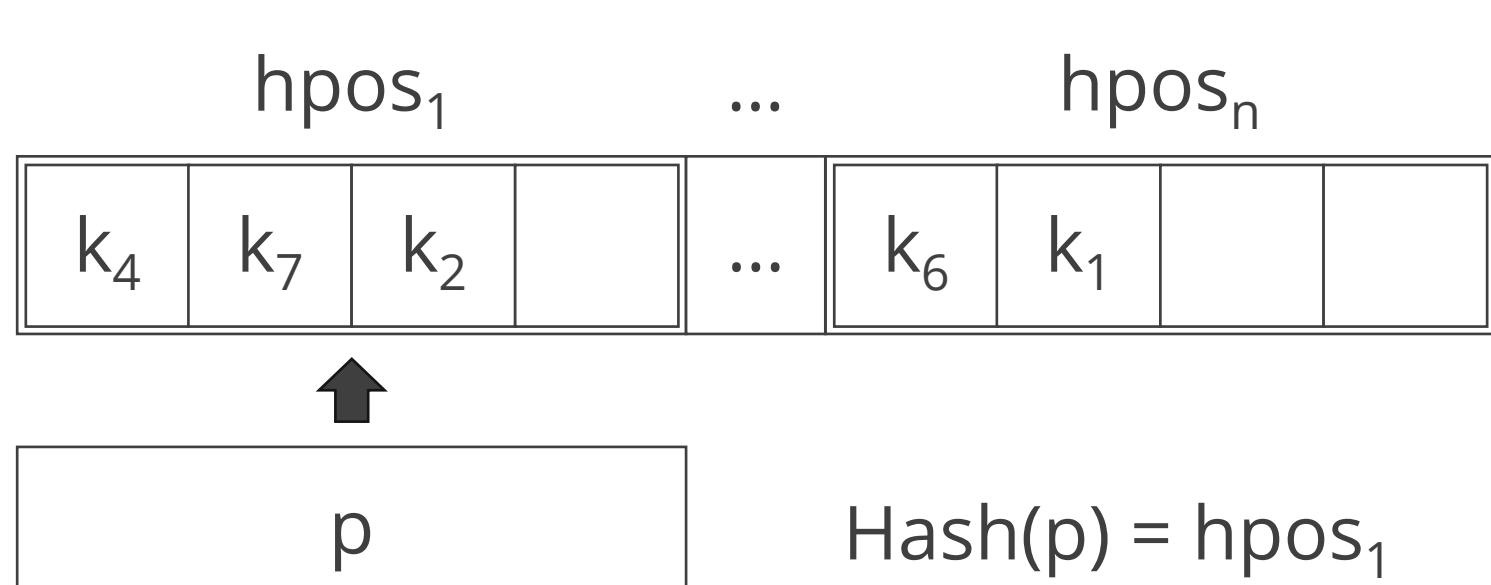
### Pipeline-Breaker Optimization – Hashing

#### Accelerating Open Addressing with SIMD

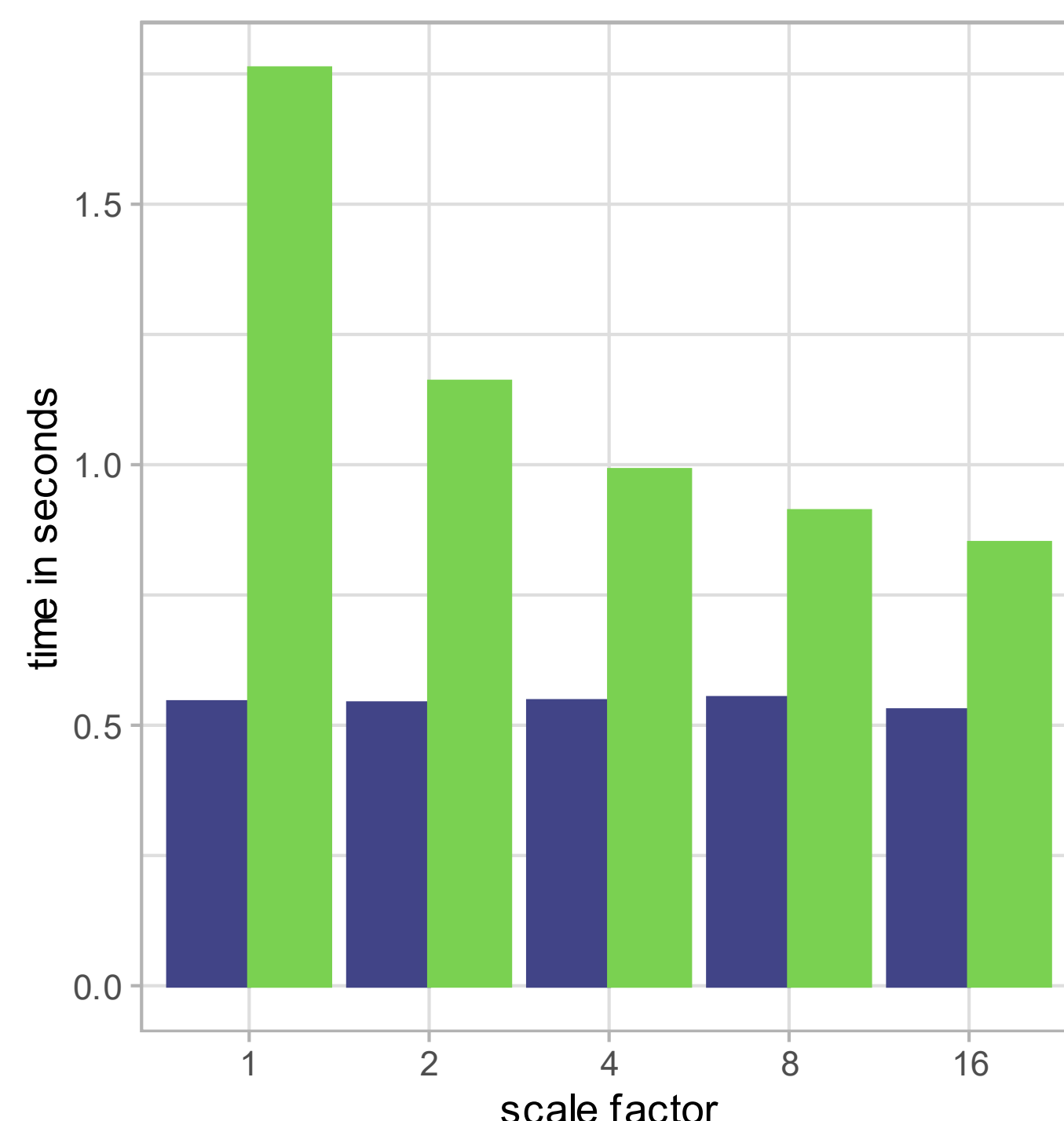
SIMDified Data Access (LP horizontal)



SIMDified Data Structure (LCP)



10240 Distinct Values 5120 Collisions



Algorithm: LCP LP horizontal

### New System under Test

#### 2x Intel Xeon CPU Max 9468

per Socket:

- 48 cores (96 threads)
- 8 channel DDR 5-DRAM
- 4 HBM2e-devices
- 4 DSA-devices (DMA-engines)

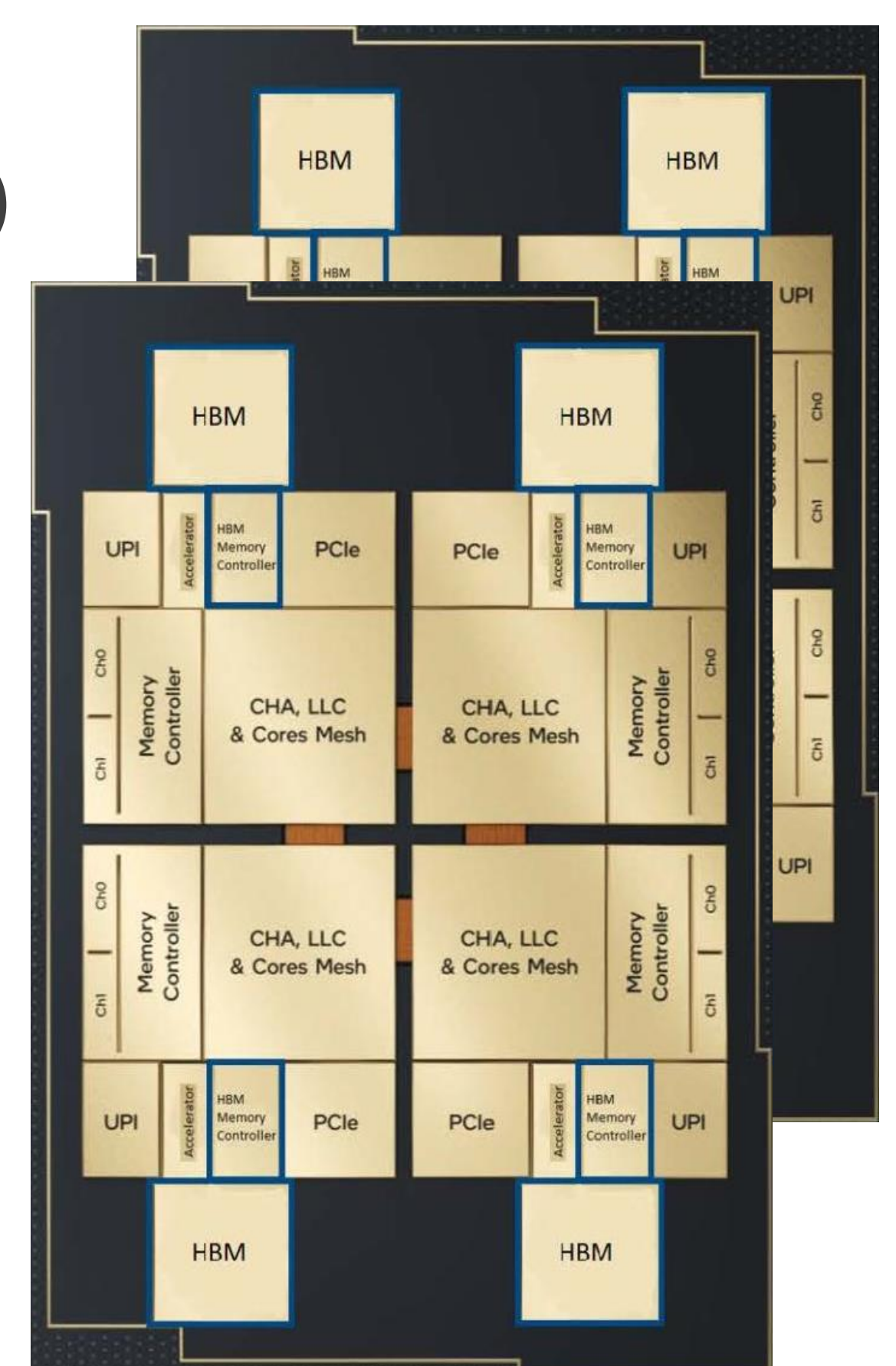


Image reference: P. Kennedy, "Intel Xeon Max CPU is the Sapphire Rapids HBM Line". servethehome.com. <https://www.servethehome.com/intel-xeon-max-cpu-is-the-sapphire-rapids-hbm-line/>. (accessed Aug. 13, 2023)